# GR 800 S2 64 L6 2G

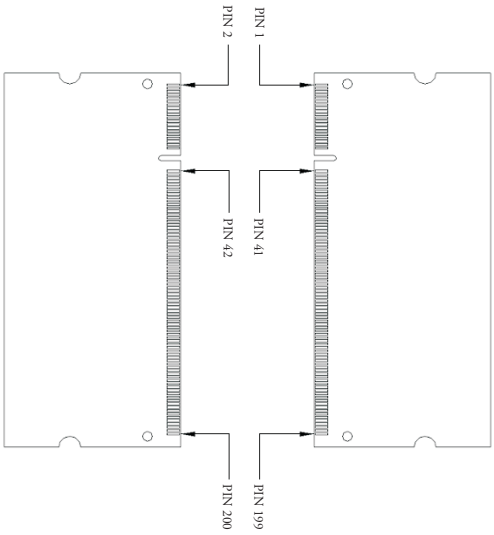
- GR — GOODRAM
- 800 — SPEED / DATA TRANSFER 800MHz / PC2-6400
- S2 — MODULE TYPE DDR2 SO-DIMM
- 64 — MODULE DATA WIDTH 64
- L6 — CAS LATENCY 6
- 2G — MODULE DENSITY 2GB

**DDR II MODULE PART NUMBERING SYSTEM**

GOOD RAM
professional memory for everyone

## FEATURES

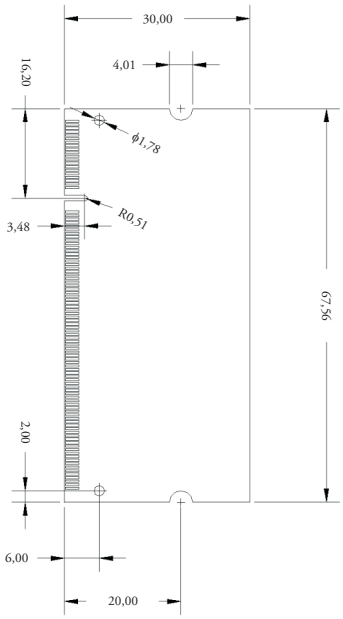
| | |
|---|---|
| PART NUMBER | GR800S264L6/2G |
| MODULE TYPE | DDR2 SDRAM SODIMM |
| MODULE DENSITY | 2GB |
| MODULE DATA WIDTH | 64 |
| DRAM CHIP ORAGNIZATION | 128Mx8 |
| NUMBER OF DRAM CHIPS | 16 |
| NUMBER OF MODULE RANKS | 2 |
| NUMBER OF MODULE SIDES | 2 |
| REGISTERED | NO |
| ECC SUPPORT | NO |
| PIN COUNT | 200 PIN |
| SUPPLY VOLTAGE | 1,8V |
| SSTL_18 COMPATIBLE | YES |
| PROGRAMMED SPD MEMORY | 128 BYTES |
| MAX AVG PERIODIC REFRESH INTERVAL | 7,8 µs |




| OPERATING FREQUENCY | CAS Latency |
|---|---|
| 800MHz (2x400MHz) \| PC2-6400 | 6 |
| 667MHz (2x333MHz) \| PC2-5300 | 5 |
| 533MHz (2x266MHz) \| PC2-3200 | 4 |

## DYNAMIC PARAMETERS FOR 800MHz

| | |
|---|---|
| RAS# TO CAS# DELAY, tRCD | 15 ns |
| ROW PRECHARGE TIME, tRP | 15 ns |
| ROW ACTIVE TO ROW ACTIVE DELAY, tRRD | 7,5 ns |
| ACTIVE TO PRECHARGE TIME, tRAS | 45 ns |
| ACTIVE TO ACTIVE / AUTO REFRESH TIME, tRC | 57 ns |
| AUTO REFRESH TO ACTIVE / AUTO REFRESH, tRFC | 127 ns |
| DEVICE CYCLE TIME, tCK MAX | 8 |




## PCB DETAILS

| | |
|---|---|
| PCB TYPE | DDR2 SDRAM SODIMM |
| BOARD DIMENSIONS | 67,56 x 30mm ± 0,1mm |
| BOARD THICKNESS | 1,27mm ± 0,13mm |
| DRAM PACKAGE INFORMATION | FBGA, x8bit |
| CONTACT PADS (PIN) | GOLD PLATED |

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Rev. 10.07.2008

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## SPD CONFIGURATION

| BYTE | DESCRIPTION | HEX | DEC |
|---|---|---|---|
| 0 | Number of Serial PD Bytes written during module production | 0x80 | 128 |
| 1 | Total number of Bytes in Serial PD device | 0x08 | 8 |
| 2 | Fundamental Memory Type (FPM, EDO, SDRAM ...) | 0x08 | 8 |
| 3 | Number of Row Addresses on this assembly | 0x0E | 14 |
| 4 | Number of Column Addresses on this assembly | 0x0A | 10 |
| 5 | Number of DIMM Banks | 0x61 | 97 |
| 6 | Data Width of this assembly | 0x40 | 64 |
| 7 | Data Width of this assembly | 0x00 | 0 |
| 8 | Voltage Interface Level of this assembly | 0x05 | 5 |
| 9 | SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X | 0x25 | 37 |
| 10 | SDRAM Access from Clock | 0x40 | 64 |
| 11 | DIMM configuration type (Non-parity, Parity or ECC) | 0x00 | 0 |
| 12 | Refresh Rate/Type | 0x82 | 130 |
| 13 | Primary SDRAM Width | 0x08 | 8 |
| 14 | Error Checking SDRAM Width | 0x00 | 0 |
| 15 | SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back RCA | 0x00 | 0 |
| 16 | SDRAM Device Attributes: Burst Lengths Supported | 0x0C | 12 |
| 17 | SDRAM Device Attributes: Number of Banks on SDRAM Device | 0x08 | 8 |
| 18 | SDRAM Device Attributes: CAS Latency | 0x70 | 112 |
| 19 | SDRAM Device Attributes: CS Latency | 0x01 | 1 |
| 20 | SDRAM Device Attributes: Write Latency/DIMM Type Information | 0x04 | 4 |
| 21 | SDRAM Module Attributes | 0x00 | 0 |
| 22 | SDRAM Device Attributes: General | 0x07 | 7 |
| 23 | Minimum Clock Cycle at CL = X - 0.5 | 0x30 | 48 |
| 24 | Maximum Data Access Time (tAC) from Clock at CL = X - 0.5 | 0x45 | 69 |
| 25 | Minimum Clock Cycle at CL = X - 1 | 0x3D | 61 |
| 26 | Maximum Data Access Time (tAC) from Clock at CL = X - 1 | 0x50 | 80 |
| 27 | Minimum Row Precharge Time (tRP) | 0x3C | 60 |
| 28 | Minimum Row Active to Row Active delay (tRRD) | 0x1E | 30 |
| 29 | Minimum RAS to CAS delay (tRCD) | 0x3C | 60 |
| 30 | Minimum Active to Precharge Time (tRAS) | 0x2D | 45 |
| 31 | Module Bank Density | 0x01 | 1 |
| 32 | Address and Command Input Setup Time Before Clock | 0x17 | 23 |
| 33 | Address and Command Input Hold Time After Clock | 0x25 | 37 |
| 34 | Data Input Setup Time Before Clock | 0x05 | 5 |
| 35 | Data Input Hold Time After Clock | 0x12 | 18 |
| 36 | Write recovery time (tWR) | 0x3C | 60 |
| 37 | Internal write to read command delay (tWTR) | 0x1E | 30 |
| 38 | Internal read to precharge command delay (tRTP) | 0x1E | 30 |
| 39 | Memory Analysis Probe Characteristics | 0x00 | 0 |
| 40 | Extension of Byte 41 tRC and Byte 42 tRFC | 0x06 | 6 |
| 41 | SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC) | 0x39 | 57 |
| 42 | SDRAM Device Minimum Auto Refresh to Active/Auto Refresh (tRFC) | 0x7F | 127 |
| 43 | SDRAM Device Maximum device cycle time (tCKmax) | 0x80 | 128 |
| 44 | SDRAM Device Maximum skew between DQS and DQ signals (tDQSQ) | 0x14 | 20 |
| 45 | DDR SDRAM Device Maximum Read Data Hold Skew Factor (tQHS) | 0x1E | 30 |
| 46 | Reserved for future use | 0x00 | 0 |
| 47 | SDRAM Device Attributes - DDR SDRAM DIMM Height | 0x51 | 81 |
| 48 | Reserved for future use | 0x00 | 0 |
| 49 | Reserved for future use | 0x00 | 0 |
| 50 | Reserved for future use | 0x00 | 0 |
| 51 | Reserved for future use | 0x00 | 0 |
| 52 | Reserved for future use | 0x00 | 0 |
| 53 | Reserved for future use | 0x00 | 0 |
| 54 | Reserved for future use | 0x00 | 0 |
| 55 | Reserved for future use | 0x00 | 0 |
| 56 | Reserved for future use | 0x00 | 0 |
| 57 | Reserved for future use | 0x00 | 0 |
| 58 | Reserved for future use | 0x00 | 0 |
| 59 | Reserved for future use | 0x00 | 0 |
| 60 | Reserved for future use | 0x00 | 0 |
| 61 | Reserved for future use | 0x00 | 0 |
| 62 | SPD Revision | 0x11 | 17 |
| 63 | Checksum for Bytes 0-62 | 0x30 | 48 |
| 64-255 | Manufacturer's specific data | | |

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